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09/871,978	06/04/2001	Makoto Hatakenaka	401191	5265

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EXAMINER	
TON, DAVID	

ART UNIT	PAPER NUMBER
2133	9

DATE MAILED: 03/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/871,978	Applicant(s) HATAKENAKA ET AL.	
	Examiner David Ton	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-17* is/are rejected.

7)☒ Claim(s) *9 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 08/964,236.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-18 are presented for examination.

Claim Rejections - 35 USC ' 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (f) he did not himself invent the subject matter sought to be patented.

3. Claims 1-8 are rejected under 35 U.S.C. § 102(f) as being anticipated by Applicant's Admitted Prior Art (AAPA).

4. As to claim 1, AAPA [col. 1 line 45 – col. 2 line 52] discloses the invention as claimed, including a semiconductor integrated circuit device [see Fig. 12] comprising:

> A logic circuit [logic circuit 102] and a SDRAM including a core unit [SDRAM core 104], said logic circuit and said SDRAM being integrated into a single semiconductor chip [col. 1 lines 45-57]; and
>
> A SDRAM control circuit [SDRAM controller 103] receiving external control signals for said SDRAM from said logic circuit, and outputting signal to said core unit of said SDRAM [col. 1 lines 45-57], wherein the output signals from said SDRAM control circuit are internal control signals for controlling said core unit of said SDRAM [col. 2 lines 33-47].

5. As to claim 2, AAPA discloses the IC comprising external input terminal means [external input pin 101 of Fig. 14] and select means [two-to-one selector of Fig. 14].

6. As to claim 3, AAPA discloses the IC comprising external input terminal means [external input pin 101 of Fig. 14], synchronizing means [input synchronization latch of Fig. 14] and select means [two-to-one selector of Fig. 14].

7. As to claim 4, AAPA discloses the IC comprising external input terminal means [external input pin 101 of Fig. 14], a command decoder [command decoder of Fig. 12] and select means [two-to-one selector of Fig. 14].

8. As to claims 5 and 6, AAPA discloses the IC comprising external input terminal means [external input pin 101 of Fig. 14], synchronizing means [input synchronizing latch of Fig. 14], a command decoder [command decoder of Fig. 12] and select means [two-to-one selector of Fig. 14].

9. As to claim 7, AAPA discloses the invention as claimed, including a method for testing a semiconductor integrated circuit device [see Fig. 14], said test method including:

> A logic circuit [logic circuit 102] and a SDRAM including a core unit [SDRAM core 104], said logic circuit and said SDRAM being integrated into a single semiconductor chip [col. 3 lines 18-26]; and
>
> Providing external test signals through external input terminal means [external test pins of Fig. 13] to a selector [two-to-one selector of Fig. 14];

Providing internal control signals from a SDRAM control circuit to a selector [signals 132-136 of Fig. 14]; and

Selecting said external test signals from said external input terminal means, using said selector, for providing the selected signals to a core unit of said SDRAM for testing [see col. 3 lines 26-58].

10. As to claim 8, AAPA discloses the external test signals are internal control signals for testing said core unit of said SDRAM [col. 3 lines 18-58].

Claim Rejections - 35 USC ' 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 10-17 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Applicant's Admitted Prior Art (AAPA).

13. As to claim 10, AAPA [col. 1 line 45 – col. 2 line 52] discloses the invention substantially as claimed, including a semiconductor integrated circuit device [see Fig. 12] comprising:

A logic circuit [logic circuit 102] and a SDRAM with a command decode system [command decoder of Fig. 12] including a core unit [SDRAM core 104], said logic circuit and said SDRAM being integrated into a single semiconductor chip [col. 1 lines 45-57]; and

A SDRAM control circuit [SDRAM controller 103] receiving external control signals for said SDRAM with a command decode system from said logic circuit, and outputting signal to said core unit of said SDRAM [col. 1 lines 45-57], wherein the output signals from said SDRAM control circuit are internal control signals for controlling said core unit of said SDRAM with a command decode system [col. 2 lines 33-47].

AAPA does not explicitly teach the SDRAM testing can be applied to other type of RAM testing.

However, it would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to apply the SDARM testing taught by AAPA for testing of any type of RAM whose is incorporated the same hardware such as a command decode system. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would enhance the application of AAPA.

14. As to claims 11-15, they are similar to claims 2-6; therefore, they are rejected under the same rationale.

15. As to claim 16, AAPA teaches the invention substantially as claimed, including a method for testing a semiconductor integrated circuit device [see Fig. 14], said test method including:

A logic circuit [logic circuit 102] and a SDRAM with a command decode system including a core unit [SDRAM core 104], said logic circuit and said SDRAM being integrated into a single semiconductor chip [col. 3 lines 18-26]; and

Providing external test signals through external input terminal means [external test pins of Fig. 13] to a selector [two-to-one selector of Fig. 14];

Providing internal control signals from a SDRAM with a command decode system to a selector [signals 132-136 of Fig. 14]; and

Selecting said external test signals from said external input terminal means, using said selector, for providing the selected signals to a core unit of said SDRAM with a command decode system for testing [see col. 3 lines 26-58].

AAPA does not explicitly teach the SDRAM testing can be applied to other type of RAM testing.

However, it would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to apply the SDARM testing taught by AAPA for testing of any type of RAM whose is incorporated the same hardware such as a command decode system. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so because it would enhance the application of AAPA.

16. As to claim 17, it is similar to claim 8; therefore, it is rejected under the same rationale.

17. Claims 9 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton, whose telephone number is (703) 306-3043. The examiner can normally be reached Monday through Thursday from 6:30 AM to 4:00 PM and alternate Friday from 6:30 AM to 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached at (703) 305-9595.

Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: (703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

DAVID TON
PRIMARY EXAMINER

DT

March 19, 2004